Final Exam

Question: 1

(a) Comparison between FETs and BJTs

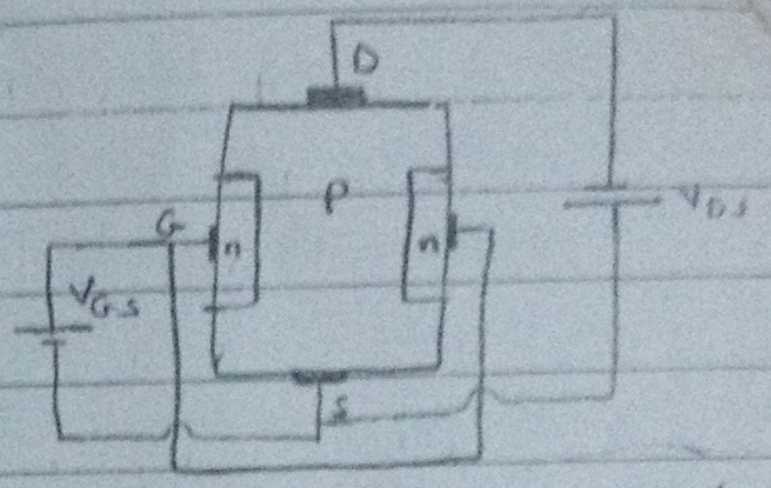
→FETs←

- the FET is a unipolar device, which depends on only one type of charge carriers, either electrons or holes, or by other mean, the current is conducted by one type of charge carriers flowing through one type of S.C.
- the FET is voltage controlled, i.e. an i/p voltage controls an o/p current
- the i/p impedance is extremely high (MΩ) and therefore they require very little power from the driving source (so they are preferred over BJTs)
- the FET is simpler to fabricate and occupies less space in integrated form (so they are preferred over BJT to be used in integrated Form)

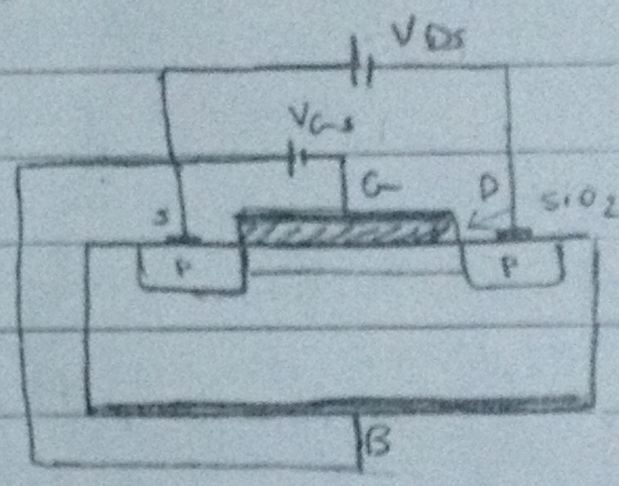
→BJTs←

- the BJT is a bipolar device, which depends on both types of charge carriers
- the BJT is current controlled, i.e. an i/p current controls an o/p current
- the i/p impedance is smaller than FET
- the BJT occupies a larger space in integrated form

(b) For a JFET, the channel gate p n junction is reverse bi so that the current is prevented to flow in the gate terminal



• For a MOSFET (either D-MOSFET or E-MOSFET) the gate is insulated from the channel, so that the current is prevented to flow in the gate terminal



(c) (i) at $V_{GS} = 0$ V

$V_{DS(P)} = V_{GS} - V_P$ ∴ $V_P = -4$ V

$I_{DSS} = 16$ mA $V_{GS(OFF)} = V_P = -4$ V

(ii) $V_{GS} = -2$ V

$V_{DS(P)} = V_{GS} - V_P$

$4 = -2 - V_P$ $V_P = -6$ V $= V_{GS(OFF)}$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ ∴ $16 = I_{DSS}\left(1 - \frac{-2}{-6}\right)^2$

$I_{DSS} = 36$ mA

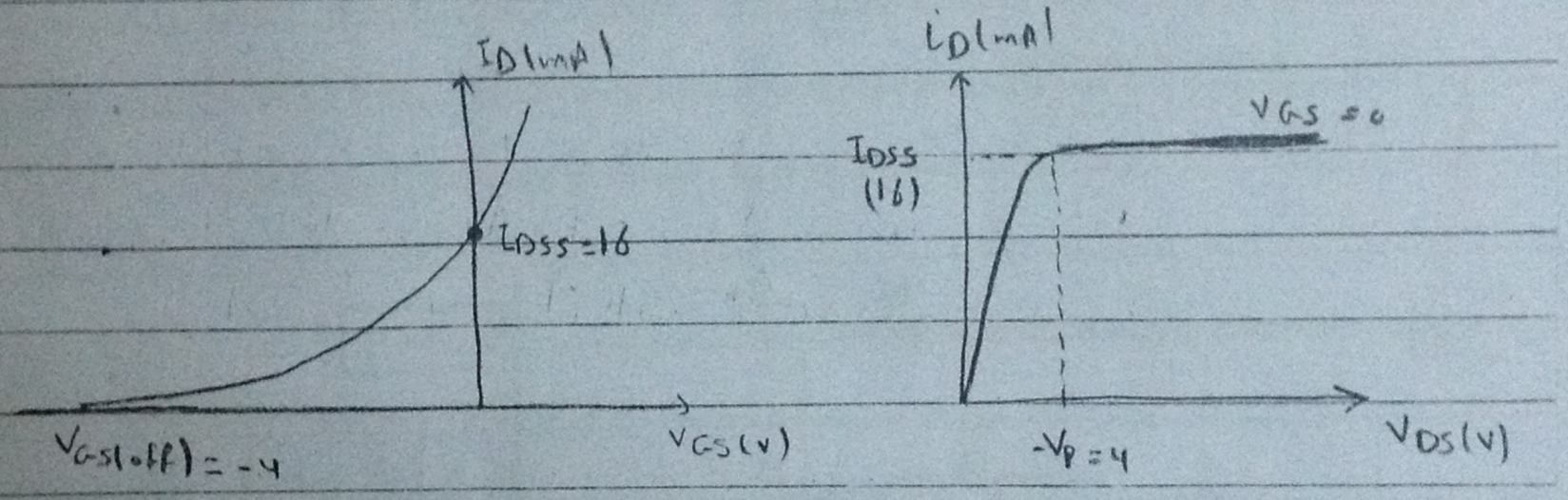
$V_{GS} = 2\ V$

$V_{DS(P)} = V_{GS} - V_P$

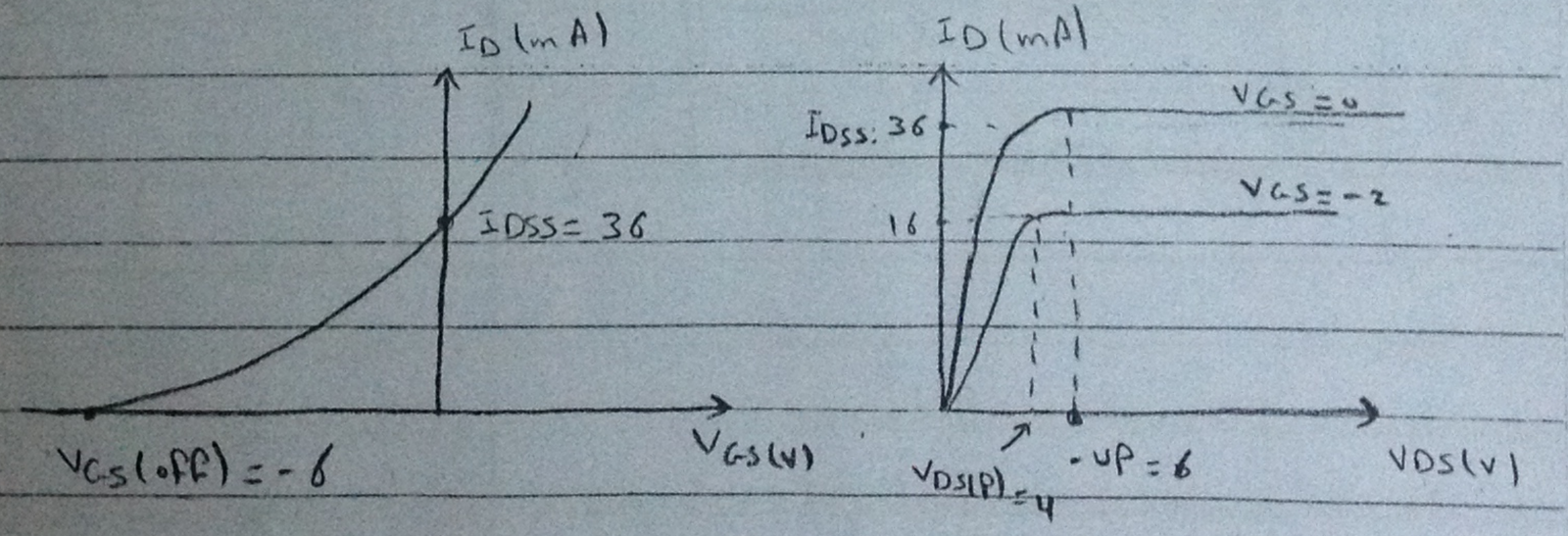
$4 = 2 - V_P$ $\quad \therefore V_P = -2\ V = V_{GS(off)}$

$16 = I_{DSS}\left(1 - \frac{2}{-2}\right)^2$ $\quad \therefore I_{DSS} = 4\ mA$

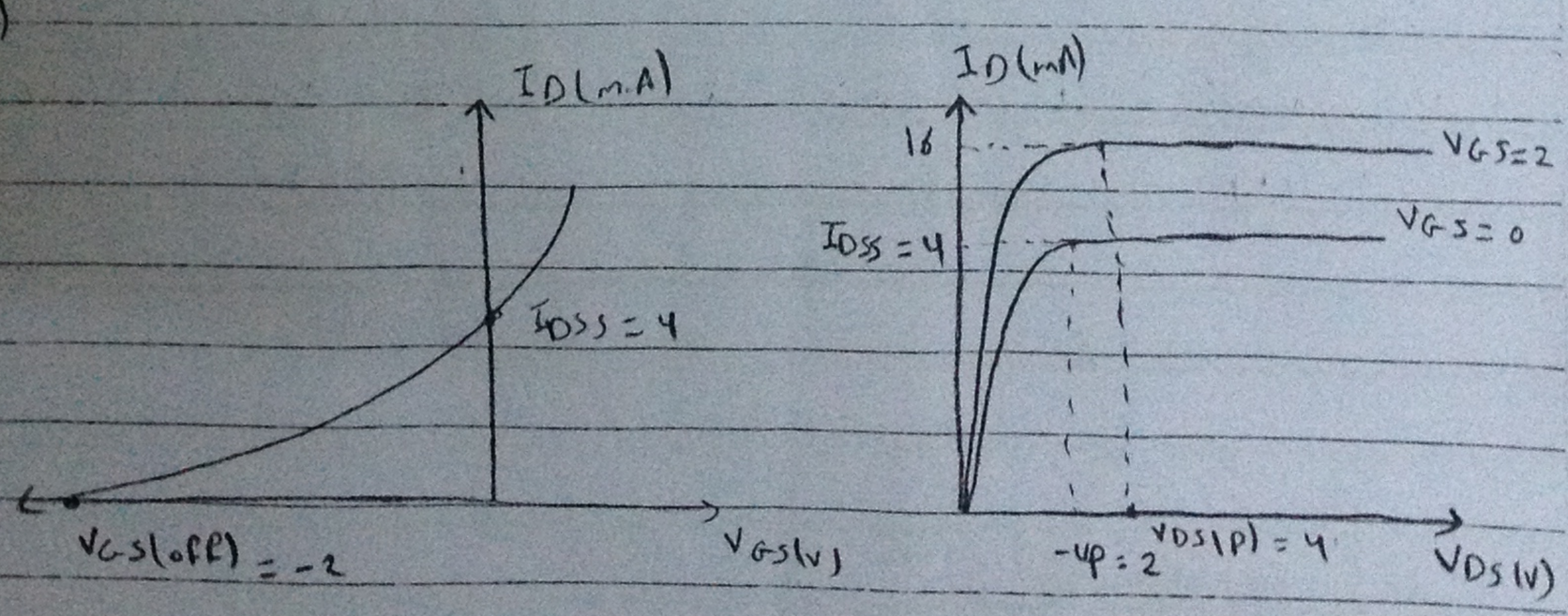
(ii) Case (A)



Case (B)



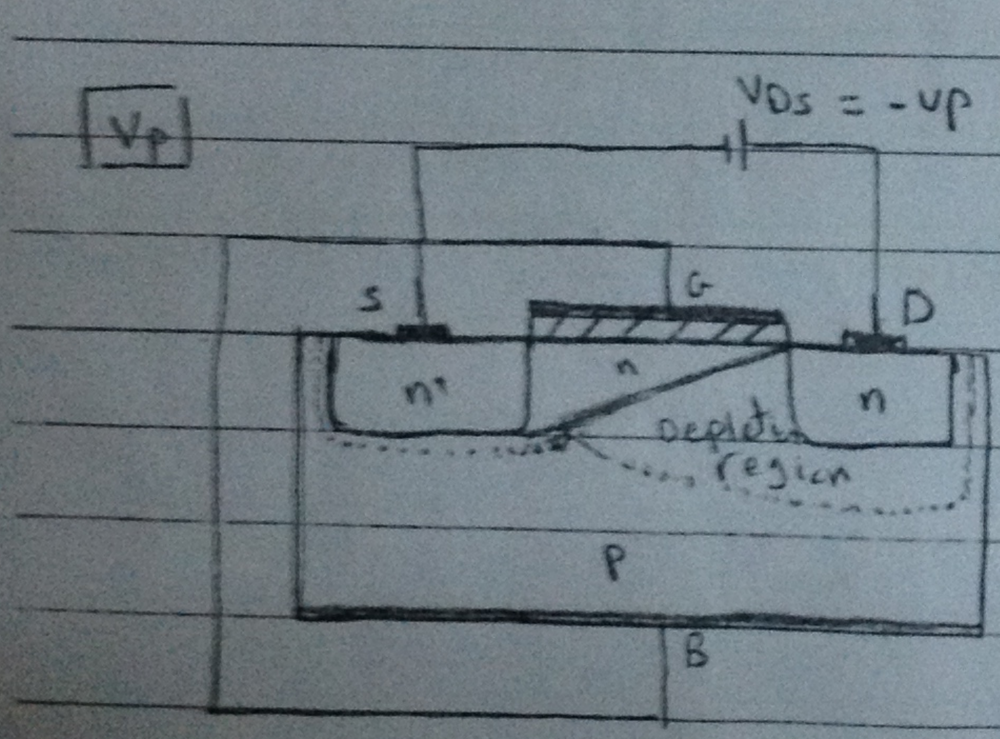
Case (C)



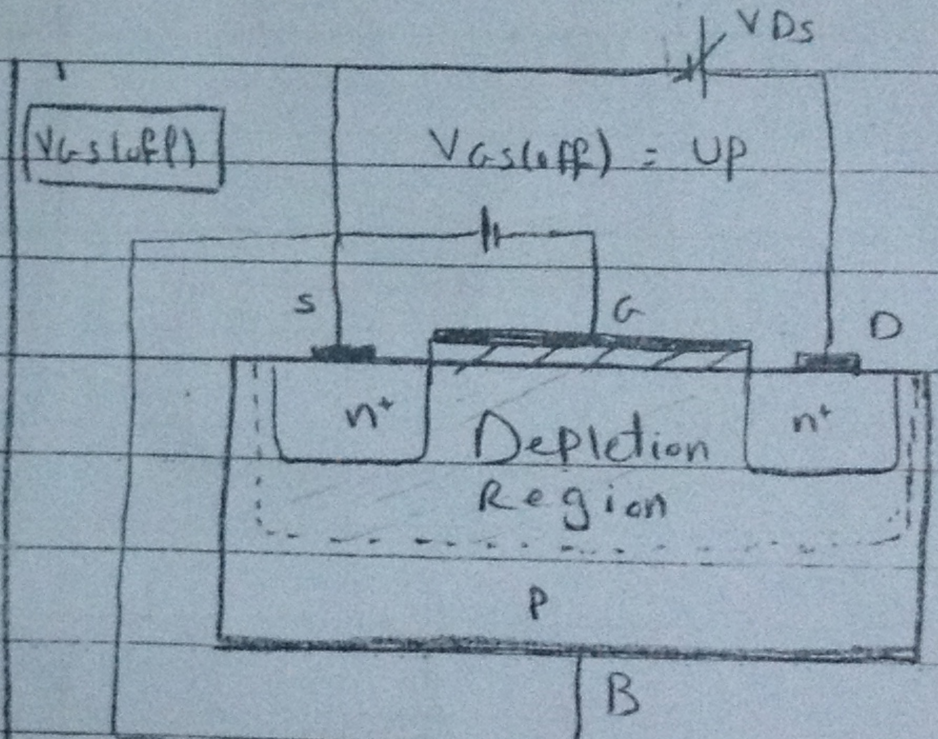
(iii) I_{DSS} is the saturation current passes through the channel when $V_{GS} = 0$ and $V_D = -V_P$

V_P is the value of V_{DS} at which the channel is Pinched at the drain end only when $V_{GS} = 0$ and the current is I_{DSS}

$V_{GS(off)}$ is the value of V_{GS} at which the channel is completely Pinched off and is entirely depleted of charge carriers, hence no current will flow ($i_D = 0$)



* $V_{GS} = 0$
* $I_D = I_{DSS}$
* the channel is pinched off at drain end only



* $V_{GS(off)} = V_P$
* $I_D = 0$
* the channel is completely Pinched-off

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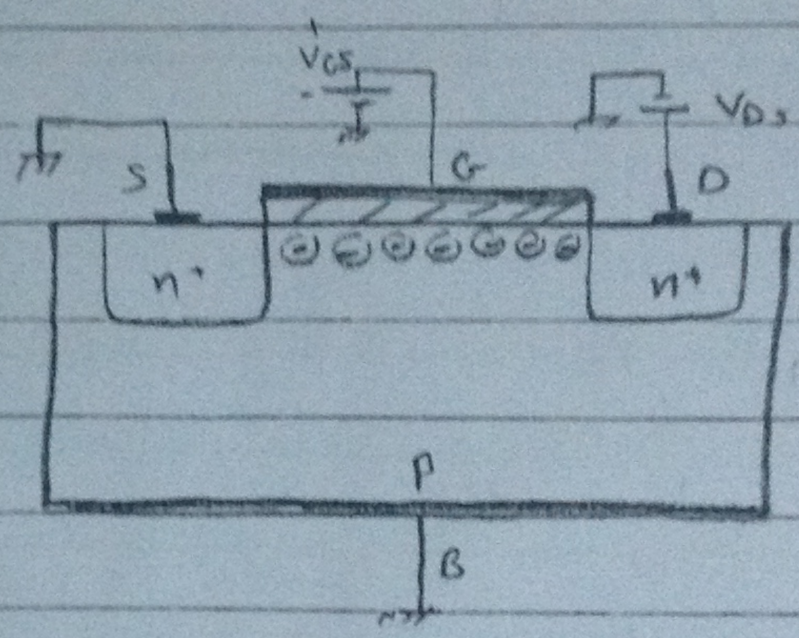
Question : 2

(a) (i) the FET is E-MosFET
and the drain current does not flow because $V_{GS} < V_t$

(ii) steps.

* at the beginning, when +ve voltage on the gate deposits +ve charges on the metal and calls for a corresponding net -ve charge at the surface of the S.C, such a -ve charge in a P type material arises from depletion of the holes from the region near the surface

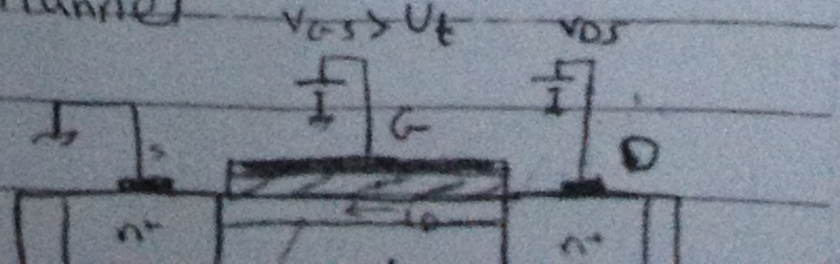


these holes are pushed downward into the substrate, leaving behind a carrier depletion region

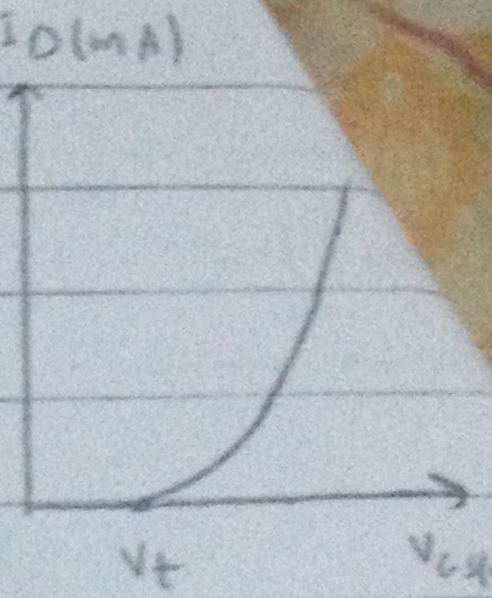
* (if V_{GS} is made more +ve), this will attract more electrons from the n^+ source and drain regions into the surface of the substrate under gate

* when a sufficient number of electrons accumulates in the channel region, an n region is induced connecting source and drain region

* this value of V_{GS} is called (V_t) and it must be exceeded for current to to follow through the induced channel



(iii) Transfer chics

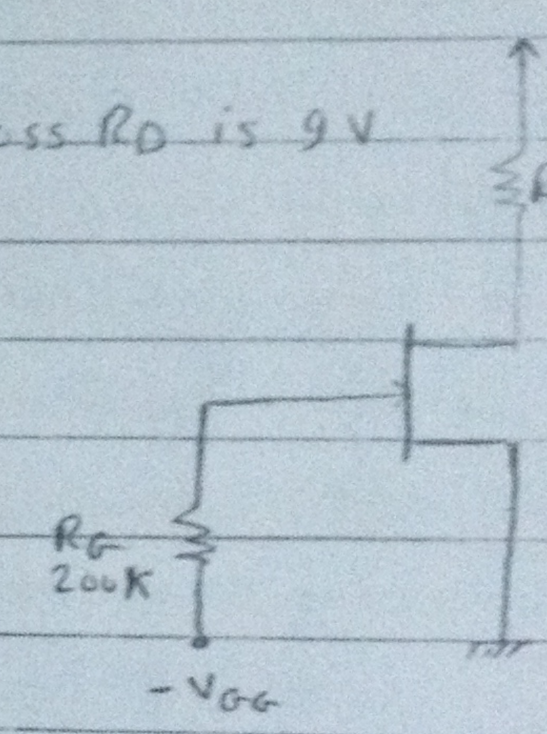


V_t : the value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel

(b)

(i) $V_{GS} = -2V$, $V_{DG} \geq 12V$, the volt across R_D is 9 V

$$I_D = \frac{V_{R_D}}{R_D} = \frac{9}{1} = 9mA$$



∴ For $V_{DG} \geq 12V$, i_D is const at 9 mA

$\therefore V_P = -12V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$9 = I_{DSS}\left(1 - \frac{-2}{-12}\right)^2 \quad \therefore I_{DSS} = 12.96\ mA$$

$V_{GS(off)} = V_P = -12V$

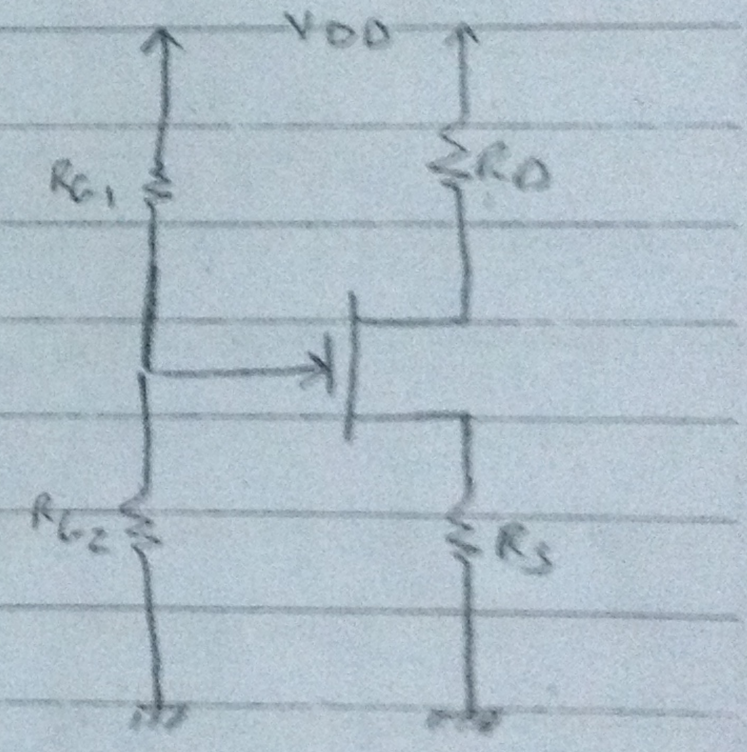
(ii) R_G is taken large to isolate the gate from ground for ac singnals

(iii) this type of biasing can be used to biass all types of FET because it provide the appropriate value of V_{GS}, but with E-MOSFET we must connect the gate termind with the +ve polarity of the V_{GG} source

it is not preferable to use this technique fo biasing FETs because it is not a stable biasing technique, since the chics of the individual FETs used in mass production may vary over a wide range, thus for some circuits, the amount of V_{GS} may provide a very large drain current, whereas in other circuits the same value of V_{GS} might reduce the drain current to near zero

* a Preferable biasing technique is (Voltage divider Bias)

this technique is a stable one as it minimizes the variance in I_D between different FET devices



* For JFET and D-MOSFET,
R_S is a self bias resistance and also acting as feedback resistance

but for E-MOSFET:
R_S is not self-bias resistance and its role is to provide -ve feedback that stablizes the dc operating point

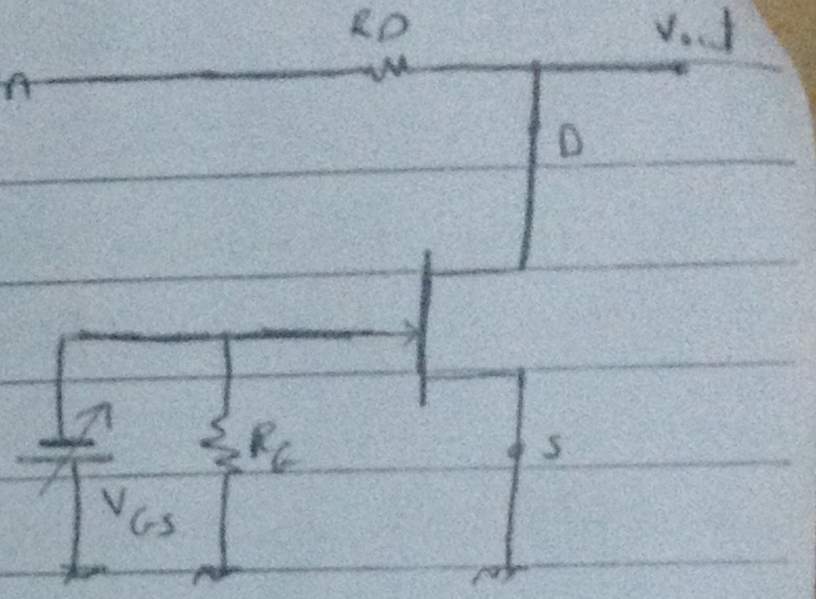
(8)

Question: 3

(a) FET applications:

* analog application:

Analog switch



- when no gate voltage is applied to the FET i.e $V_{GS} = 0$, the FET becomes saturated and behave like a small resistance usually of value less than 100 Ω and o/p voltage.

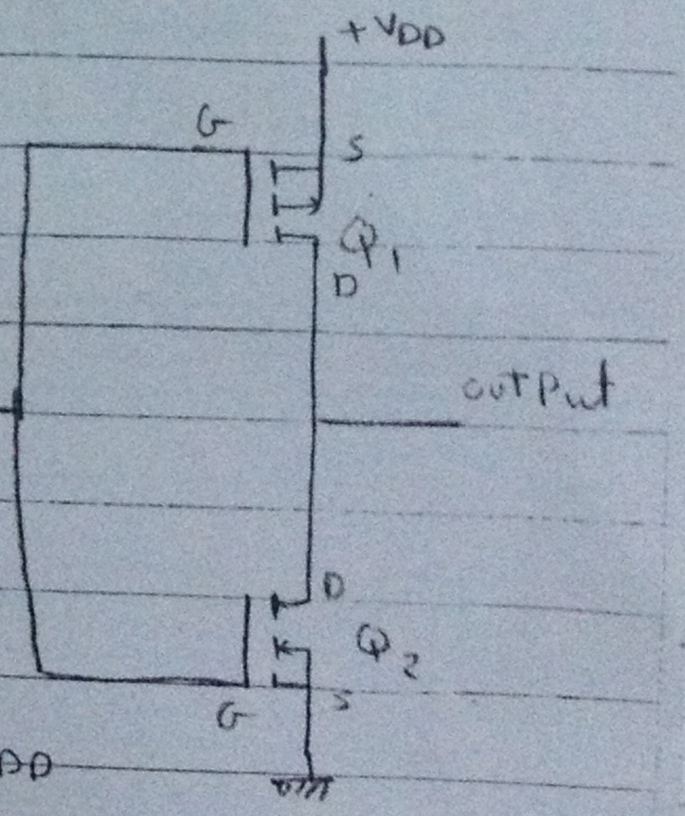
$$V_{out} = \frac{R_{DS(on)}}{R_D + R_{DS(on)}} V_{in}$$

since $R_D \gg R_{DS(on)}$, so V_{out} can be taken equal to zero

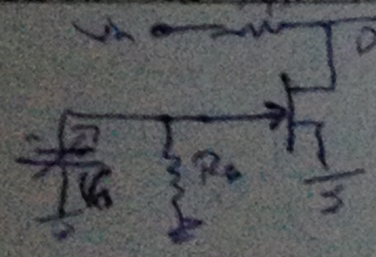
- when a -ve voltage equal to $V_{G(off)}$ is applied to the gate the FET operates in the cut-off region and acts as a very high resistance usually of some mega ohm, hence the o/p voltage becomes equal to input voltage

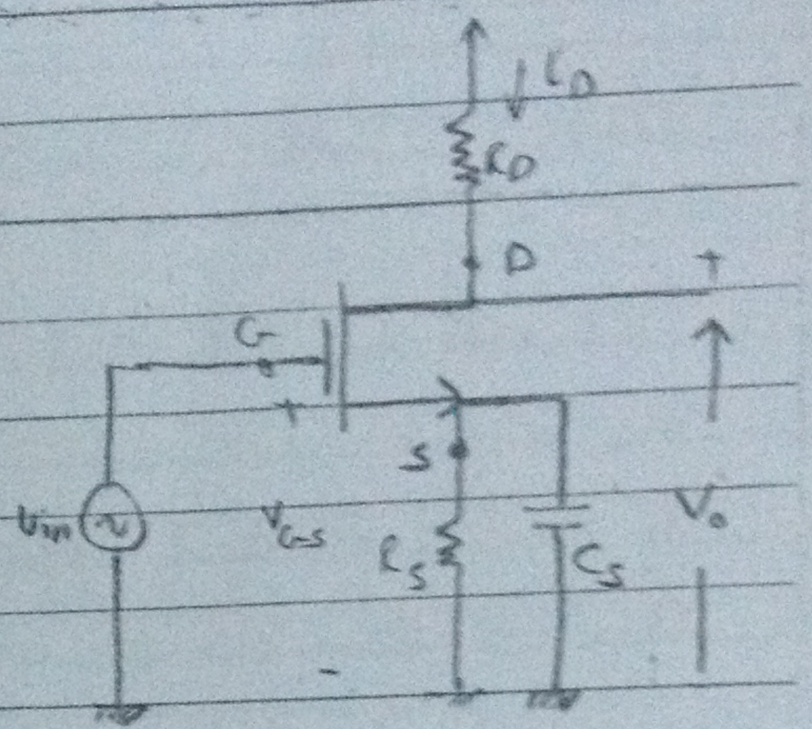
* digital applications *

CMOS Inverter

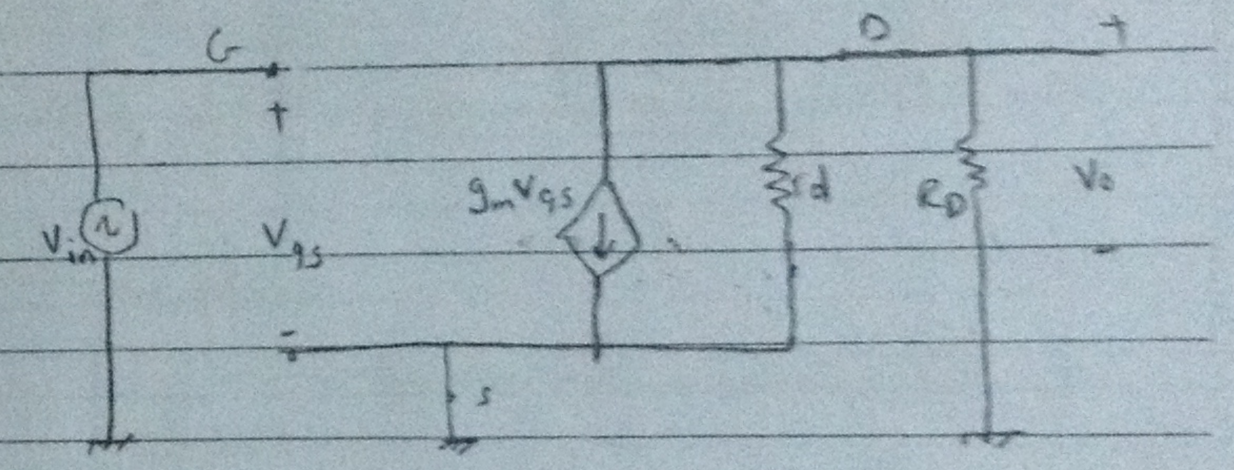


- when a High is applied to the input, Q_1 is off and Q_2 is on, this condition connects the o/p to ground through the on resistance of Q_2 resulting in a low o/p
- when a low is applied to the i/p, Q_1 is on and Q_2 is off, this condition connects the o/p to $+V_{DD}$ through the on resistance of Q_1 resulting in a high o/p





* linear equivalent model



$$V_{gs} = V_g - V_s$$
$$= V_i - 0 = V_i$$

$$V_o = -g_m V_{gs} \left(\frac{r_d R_D}{R_D + r_d} \right)$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m r_d}{1 + r_d / R_D} = \frac{M}{1 + r_d / R_D}$$

(c) For a common source FET amplifier using the high freq small signal model: the i/p admittance.

$$y_i = \omega C_{gd} A_x + j\omega [C_{gs} + (1 - A_R) C_{gd}] = R_i + j\omega C_i$$

in general, A_R will be a relatively large negative number so C_i will be much larger than might be expected from the values of C_{gs} and C_{gd}. this increase in capacitance is called Miller effect, in general it is desirable for the i/p admittance to be small, therefore C_{gs} and C_{gd} should both be small during FET Fabrication.

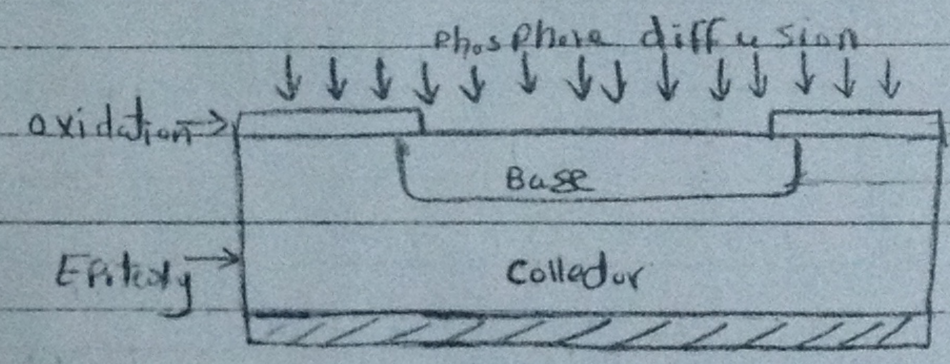
-and also this effect can be diminished, if $|A_R|$ were small.

Question: 4

steps to fabricate a BJT :

1. A lightly doped layer of N-type material is epitaxially grown on a p^+ wafer the n^- S.C will constitute the collector material, the p^+ support can be used to provide efficient device isolation when the device is used in I.C this isolation can be achieved by applying a strong -ve bias to the p^+ S.C.

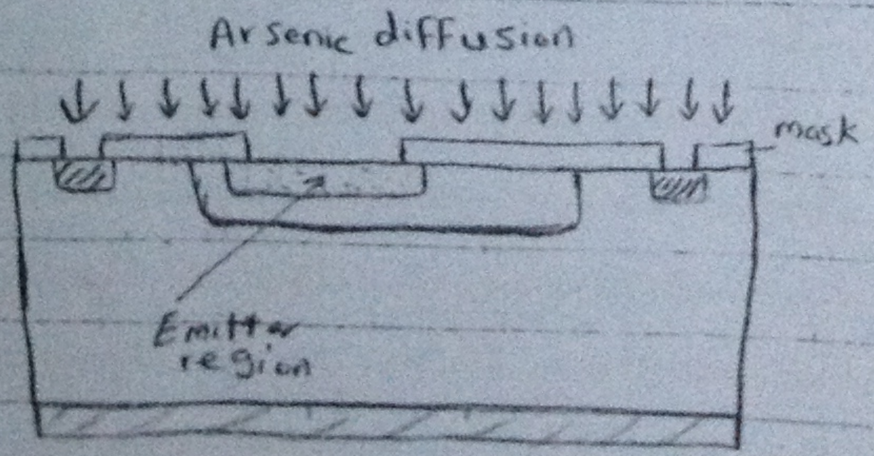
2. the wafer surface is oxidized, and using photolithographic step to create the appropriate mask, a p- layer (the base region is diffused in the n^- material



3. the oxide layer is stripped away and a new layer is grown, usually by wet oxidation process

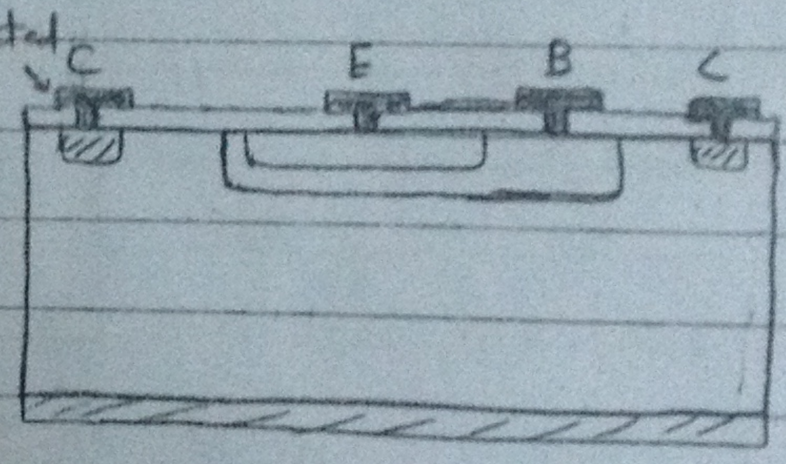
4. using a photolithography another mask is created that expose the S.C material at the proper positions for diffusion of the emitter and of the collector contact regions

5. by either diffusion or ion implantation, shallow heavily doped n and n^+ regions are fabricated, they are the emitter and omic contact regions of the collector



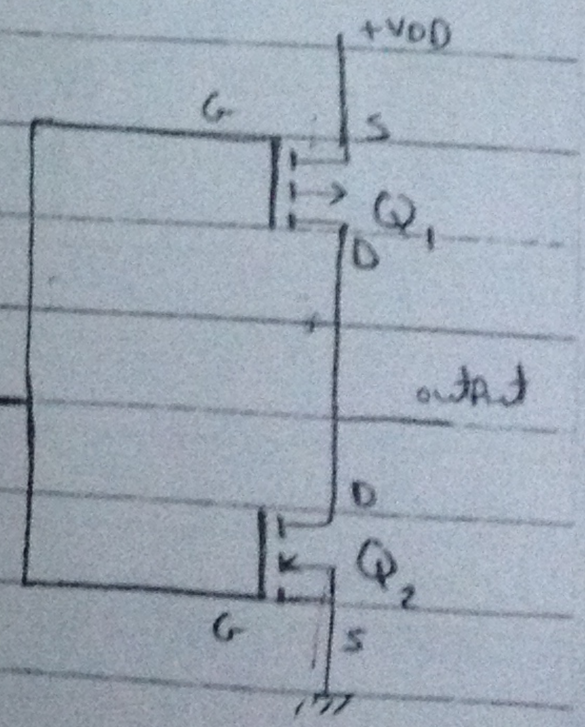
the oxide layer is stripped away and a new oxide coating is grown, than using photolithography another mask is created that have wells opened in the oxide to permit contact with the various regions of the transistor

7- the whole face of the wafer is metallized and using another mask, the metal is etched to yield the desired electrode configuration. shaw in the figure below



Question: 5

(1) CMOS inverter



- when a HIGH is applied to the i/p, Q_1 is off and Q_2 is on, this condition connects the o/p to ground through the on resistance of Q_2 resulting in a Low o/p
- when a LOW is applied to the i/p, Q_1 is on and Q_2 is off, this condition connects the o/p to +VDD through the on resistance of Q_1 resulting in a high o/p

- this continues until the ...
- I-V characteristics approaches that of ...
- An ...

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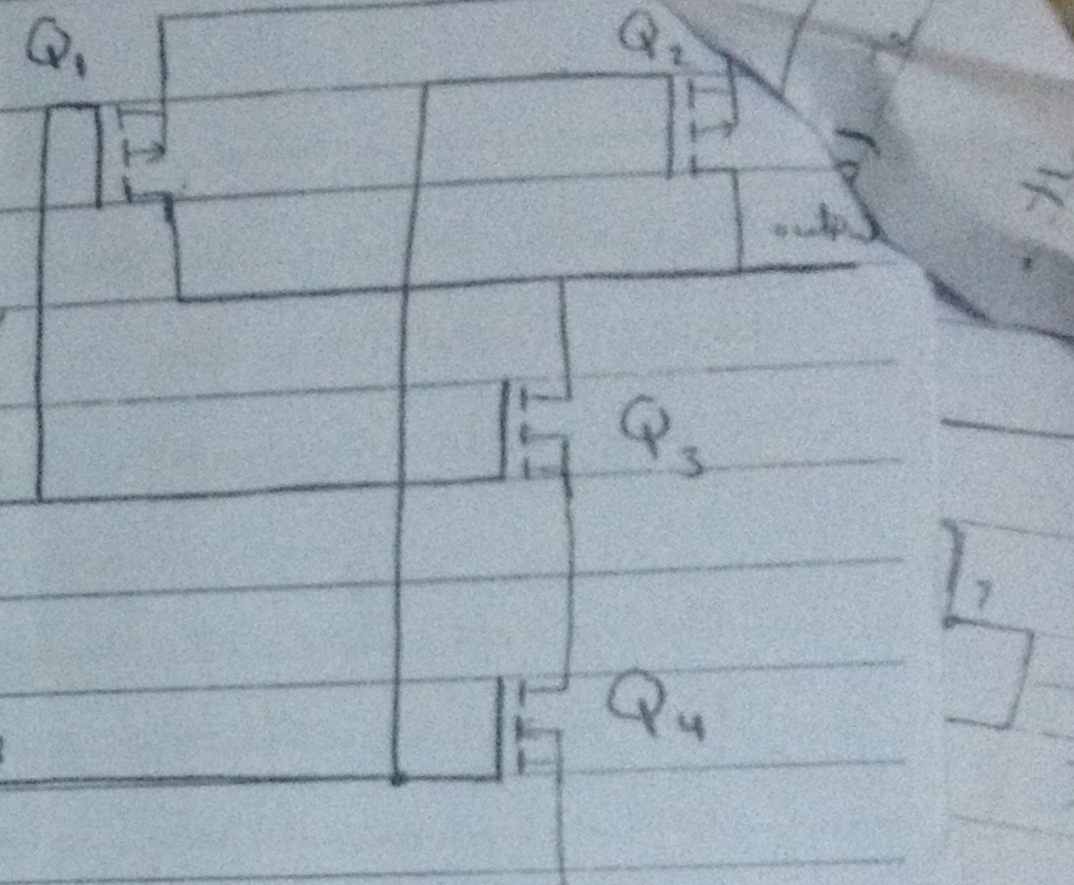
(ii) CMOS NAND Gate.



- when both i/Ps are low, Q_1 and Q_2 are on, and Q_3 and Q_4 are off. the o/P is pulled HIGH through the on resistance of Q_1 and Q_2 in parallel

- when input A is Low and input B is HIGH, Q_1 and Q_4 are on, and Q_2 and Q_3 are off, the o/p is pulled High the low on resistance of Q_1

- when input A is High and input B is low, Q_1 and Q_4 are off, and Q_2 and Q_3 are on, the o/p is pulled High through the on resistance of Q_2

- finally, when both i/Ps are HIGH, Q_1 and Q_2 are off, and Q_3 and Q_4 are on. in this case, the o/p is pulled Low through the on resistance of Q_3 and Q_4 in series to ground

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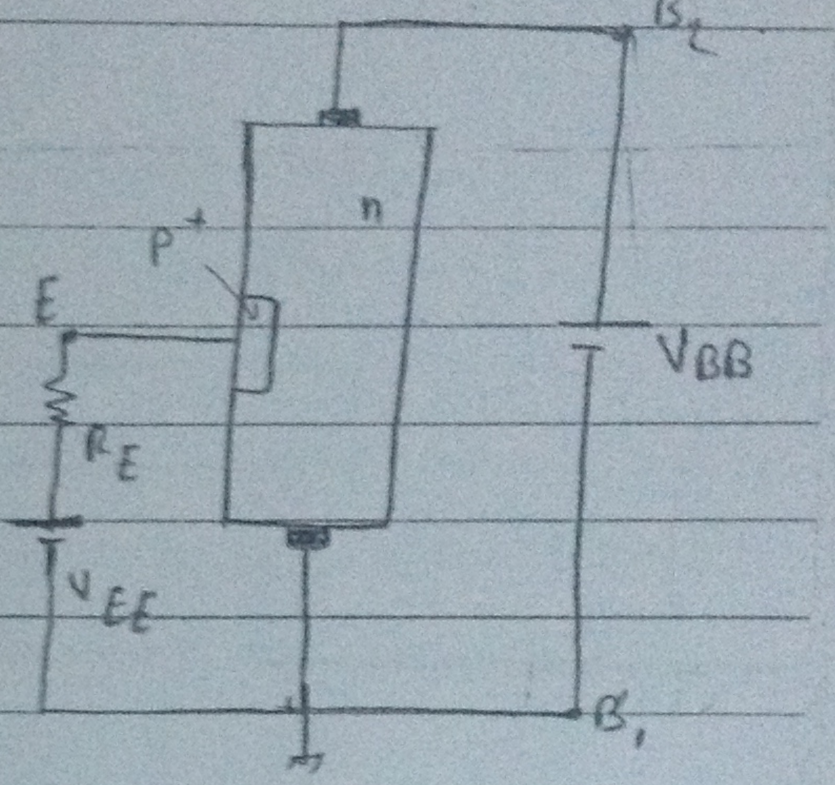
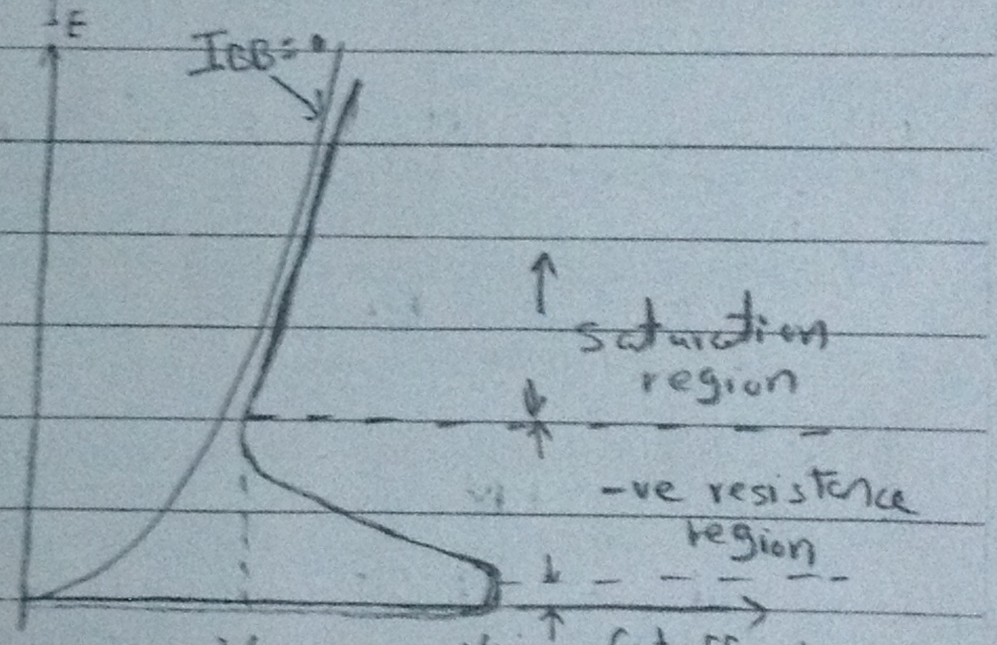
(20) the unijunction Transistor:



- the UJT has a high impedance in the off state and a low impedance in the on state and is switched from one state to another by a mechanism called (conductivity modulation)

- if $I_{BB} = 0$, the I-V chics is that of ausual p-n junction

- if B_2 is not left open, the I-V chics are different as shown



- For small V_E, the s.c bar has afixed resistance $R_{BB} = R_{B_1} + R_{B_2}$ between B_1 and B_2

- if V_E is increased, so that V_E exceeds V_p - , the Emitter Junction becomes Forward biased and holes are injected From the p^+ Emitter into the n- region

- The excess holes in the n-region will tend to increase its conductivity, leading To a slight reduction in R_{B_1} (this is what is known as (conductivity modulation)

- as aresult of the reduction in R_{B_1} and so the reduction of the voltage drop across it, the net Forward bias across the Junction increases
- This leads to an increase in I_E, which causes further conductivity increase and so Forth
- this action leads to an increase in I_E, accompained by a decrease in V_E

this continues until the drop across R_{B1} is very small and the I-V chics approaches that of a normal PN Junction

A negative resistance region is, therefore, produced in the I-V chics after the device is switched from the off state To the ON state.

Question. 7

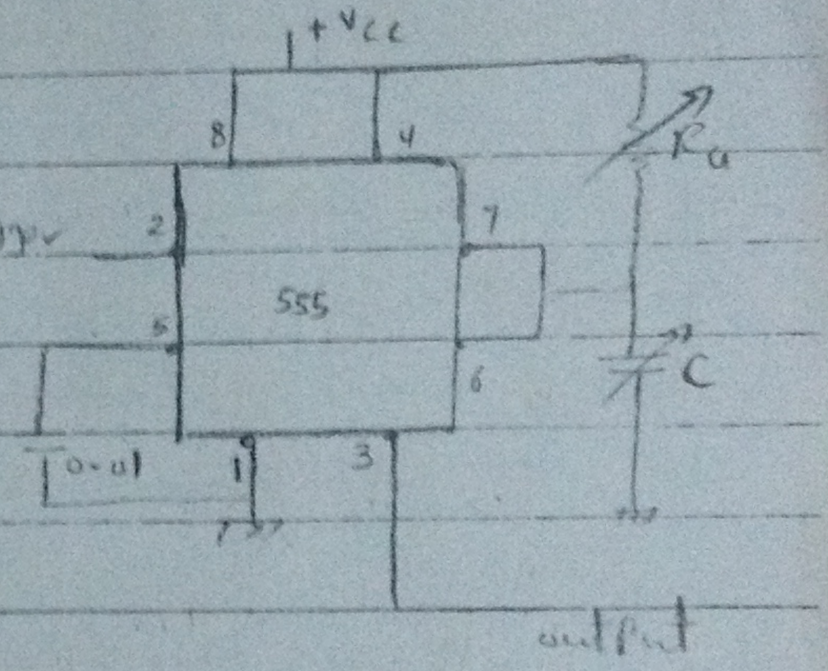
the Time width that the output is high:

$$t = 1.1(R_a)(C)$$

let $C = 1MF$ and

$R_a = 5 M\Omega$

$\therefore t = 5$ sec



timing sequence